Refine Search

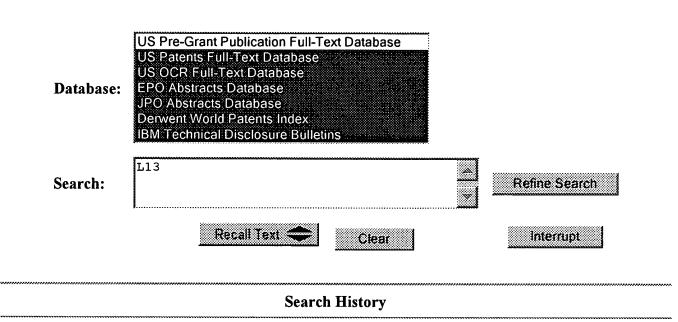
Your wildcard search against 10000 terms has yielded the results below.

Your result set for the last L# is incomplete.

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

Search Results -

Terms	Documents
L11 same test\$ same wafer	2



DATE: Wednesday, August 03, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB = USI	PT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YI	ES; OP=OR	
<u>L13</u>	L11 same test\$ same wafer	2	<u>L13</u>
<u>L12</u>	L11 and 19	1	<u>L12</u>
<u>L11</u>	L1 same 12	571	<u>L11</u>
<u>L10</u>	L9 and 11	83	<u>L10</u>
<u>L9</u>	(david near1 ton)[xa,xp]	458	<u>L9</u>
<u>L8</u>	L1 same 12 same (bist or bisr)	0	<u>L8</u>
<u>L7</u>	(4703436 5256578)![pn]	4	<u>L7</u>
<u>L6</u>	L5 same memory	6	<u>L6</u>
<u>L5</u>	L4 same test\$	68	<u>L5</u>
<u>L4</u>	L3 same 12 same 11	96	<u>L4</u>
<u>L3</u>	associat\$	2505635	<u>L3</u>

<u>L2</u>	(fail\$ near1 test) or (result adj information)	20555	<u>L2</u>
<u>L1</u>	(identif\$ near device) or id	1785322	<u>L1</u>

END OF SEARCH HISTORY

First Hit Fwd Refs

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L6: Entry 1 of 6

File: USPT

Nov 1, 1994

DOCUMENT-IDENTIFIER: US 5360747 A

** See image for <u>Certificate of Correction</u> **

TITLE: Method of reducing dice testing with on-chip identification

Detailed Description Text (6):

Referring back to FIG. 4B, during step 411, all wafers are subjected to predetermined, adverse conditions to accelerate discharge of the memory cells on the wafers. Then, in step 412 of second wafer sort 430, the probe reads the ID cells of the first electronically inked die on the wafer. For example, the probe examines the ID cells 7 (FIG. 2) on die 200 (the first electronically inked die) to access the file associated with the particular wafer on which die 200 is located, i.e. wafer W2. The file associated with wafer W2, i.e. file 2, is accessed in step 413. The probe, after reading the first location in the file, proceeds directly to the first "good" die (as determined in first wafer sort 400) on the wafer in step 414. Note that the first good die in this example is, in fact, die 200. Die 200 is then tested in step 415. If die 200 fails this test, the die is rejected, whereas if die 200 passes the test, the die is acceptable for the packaging process.

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L5: Entry 4 of 68

File: USPT

Mar 9, 2004

DOCUMENT-IDENTIFIER: US 6703573 B2

TITLE: Method for sorting integrated circuit devices

<u>Detailed Description Text</u> (5):

ICs that pass the <u>test</u> step 22 are typically shipped to customers, while those that <u>fail the test</u> step 22 are directed to the reject bin 12. At a point in time when <u>test</u> standards of the <u>test</u> step 22 have been relaxed as described above, the ICs in the reject bin 12 are sorted in a sort step 26 by reading the fuse <u>ID</u> of each IC, accessing the <u>test</u> data 24 <u>associated</u> with the fuse <u>ID</u>, and comparing the accessed <u>test</u> data 24 with the relaxed <u>test</u> standards. Those ICs that fail even the relaxed <u>test</u> standards are directed back to the reject bin 12, while those ICs that pass the relaxed <u>test</u> standards are typically shipped to customers. The method 10 thus successfully culls shippable ICs from the reject bin 12 without retesting the ICs.

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